Simple automatic-shutoff circuit uses few components

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You often need to include a timed automatic-turn-off circuit in battery-powered equipment to extend battery life. Previously published Design Ideas for this function all involve many components (**references 1** through **7**). The circuit in **Figure 1** is a simple automatic-shutoff add-on circuit featuring no quiescent current.

When you press the pushbutton switch, C_1 charges rapidly through the low-value R_2 to the zener voltage of diode D_1, and P-channel MOSFET Q_1 immediately conducts. After the pushbutton is released, C_1 discharges slowly through the high-value R_1 with a time constant of R_1C_1 seconds. During this time, C_1 loses 63% of its initial voltage—from 9V to 3V after the delay. **Reference 8** shows the on-resistance versus the gate-to-source voltage of a Vishay Siliconix Si4435. As long as the gate-to-source voltage is greater than approximately 3V, the device's on-resistance remains lower than 0.1Ω, yielding a dropout voltage of less than 0.1V for a load sinking as much as 1A.

The 9.1V zener diode, D_1, keeps the shutoff time delay independent of the battery voltage and ensures that the gate-to-source voltage does not exceed Q_1's rated maximum of 20V. Thus, you can use this circuit with a choice of battery voltages; only the maximum drain-to-source voltage of transistor Q_1 limits the choice. With 3.6 to 9V batteries, D_1 and R_1 are useless (remove D_1 and short-circuit R_2), and you must compute the time delay with the classic **equation** $T=-R_1C_1\log_e(3/V_{BAT})$, as **Table 1** shows. With battery voltages as low as 1.5V, instead use a bipolar transistor with a low saturation voltage as well as a modified circuit scheme.

Editor's note: With no feedback for rapid shutoff, as C_1 slowly discharges below 3V, Q_1 goes through a period of gradually increasing the on-resistance, which temporarily increases its power dissipation and heating during the shutoff action. Be sure to consider this effect, size Q_1 adequately for the load current, and use adequately sized heat sinks. EDN

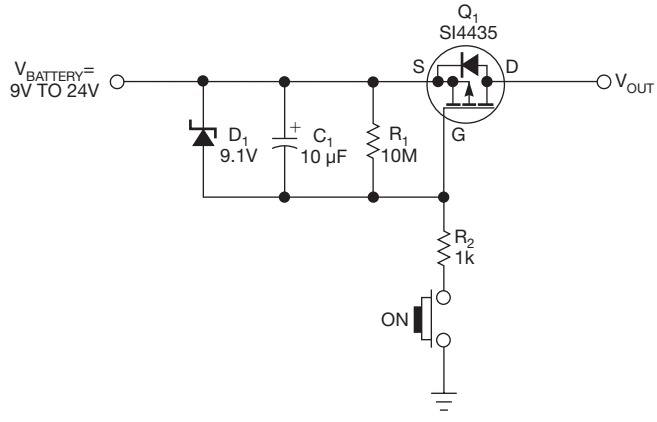

Figure 1 This simple automatic-shutoff circuit uses a P-channel MOSFET.

TABLE 1 TIME DELAY (SECONDS) WITH 10-MΩ R_1

Battery voltage (V)	LN ($3/V_{BAT}$)	C_1=10 µF	C_1=100 µF
7.5	–0.916	92	916
6	–0.693	69	693
4.5	–0.405	41	405
3.6	–0.182	18	182

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Inverting level-shift circuit has negative potential

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Digital-system designs require you to consider many core voltages. Memory operates at 1.8V, I²C and FPGA devices operate at 3.3V, microcontrollers operate at 5V, and charge-coupled-device image sensors operate at –9 to 8V. Clocks for each device must suit their operating voltages.

You can use the level-shift circuit in **Figure 1** to adjust an input clock signal to the proper logic-high and logic-low voltage levels, including negative voltages. This property is handy for devices that need a negative voltage, such as a charge-coupled-device sensor. Although the circuit's output clock is 180°-inverted relative to the input clock, that inversion does not affect the function of the device.

The level-shift circuit comprises fast-switching transistors Q_1 and Q_2. The user chooses level-shift high and level-shift low, which are dc-bias voltages and which connect to the transistor emitters, to match the desired output high- and low-logic levels. C_1, R_1, D_1, C_2, R_2, and D_2 keep the base voltages of Q_1 and Q_2 close to that of their emitters.

Because memory and charge-coupled-device sensors usually have high-frequency clocks, you can choose C_1 and C_2 to prevent low-frequency-noise pass-through. The circuit in **Figure 1** uses a 20-MHz signal for measurements (**Table 1**) and thus uses a value of 100 pF for C_1 and C_2. When the input voltage's clock is low, Q_1 turns on and Q_2 turns off, driving the output voltage's clock to the level shift's high potential. When the input voltage's clock is high, Q_1 turns off and Q_2 turns on, driving the output voltage's clock to the level shift's low potential, even when that potential is negative relative to ground.

Because of the circuit's high switching speeds, keep component leads as short as possible to minimize inductance. This caveat is especially true for C_3 through C_6's leads to their respective transistor emitters and to the ground plane or the output ground return. EDN

TABLE 1 INPUT AND OUTPUT CLOCKS

High/low level shift (V)	Input clock (V)	Output clock (V)
3.3/0	0/5	3.3/0
20/10	0/5	20/10
–5/–10	0/5	–5/–10
2/–4	0/5	2/–4

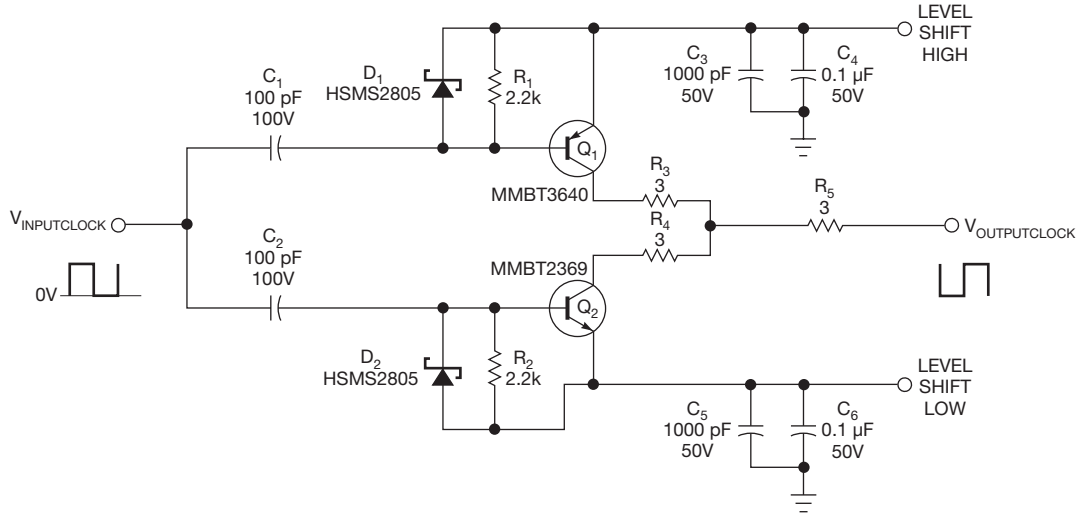

Figure 1 This simple and fast level-shift circuit can adjust an input clock to both positive and negative voltage levels.

Single hex-inverter IC makes four test gadgets

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This Design Idea describes a simple way that you can use one hex-inverter package of an unbuffered HD14069UB CMOS (**Reference 1**) to make four test gadgets: a logic probe with well-defined logic-voltage windows and with an input impedance of approximately 1 MΩ; a continuity tester whose upper limiting resistance can be tens of ohms to tens of megohms; a single or train pulse injector or a modest signal generator; and a high-impedance audio probe. You can assemble these gadgets using the six inverter gates of a 4069, two or three transistors, and a few passive components.

In a two-gate CMOS/TTL-compatible probe, the resistor network comprising R_1 through R_4 biases the inverter's inputs (**Figure 1**). Because of the gates' high input impedance, R_1 through R_4 can have values of approximately 100 kΩ to 1 MΩ. The probe's source/sink current is small at the probe tip because of the high resistances of R_1 through R_4; as a result, the probe tip essentially does not affect the logic-voltage level at the test point. Knowing the gates' input threshold voltage, you can calculate the required values of resistors R_1 through R_4.

The upper gate detects logic zero, and the lower gate detects logic one. Set an upper limit to the logic-zero voltage and calculate the values of R_1 and R_2. Arbitrarily select R_1=1 MΩ and seek a value for R_2 such that the voltage at the input of the upper gate is just the threshold voltage. Thus, $R_2=R_1(V_T-V_L)/(V_S-V_T)$, where V_T is the threshold voltage, V_L is the logic-zero voltage, and V_S is the supply voltage. Similarly, set a lower limit on the logic-one voltage V_T and seek a value for R_4 in terms of R_3. By appropriately selecting R_3, keeping in mind the quiescent biasing of the gates to keep both the LEDs off in the probe's suspended condition, you can obtain the value of R_4: $R_4=R_3V_T/(V_H-V_T)$.

The following **equation** calculates the probe current: $I_P=[-(V-V_I)(R_3+R_4)+V_I(R_1+R_2)]/(R_1+R_2)(R_3+R_4)$, where I_P is the probe current and V_I is the probe-tip voltage. It thus follows that the probe impedance for any voltage at the probe tip is greater than 1 MΩ. For packages of 4069 that exhibit a larger threshold voltage, such as 3V, you can help reduce it by including a diode followed by a 10-kΩ load resistor to ground in the positive supply rail to the chip.

Developers often use continuity testers (**Figure 2** and **Reference 2**) as elementary test gadgets; such testers are indispensable on a work bench. One of the 4069's gates, with its high input impedance and with a threshold voltage for the transition of the output of the gate, allows you to build the continuity tester with an upper limit on the resistance of the test circuit. The total of the resistance between the probes and the resistance in the switching arrangement forms a voltage-divider network, producing a voltage at the input of the gate. When the two resistances are equal, the voltage at the gate input is half the supply voltage. The transition threshold voltage of the gate is also nearly half the supply voltage; therefore, the selected resistor in the switching branch sets the approximate threshold-continuity resistance.

A useful alternative arrangement is to have a variable resistor in place of the switchable resistors. This approach allows you to set the threshold-continuity resistance arbitrarily by adjusting this resistor after including the desired resistance between the probe tips and observing the LED's glow. The variable resistor

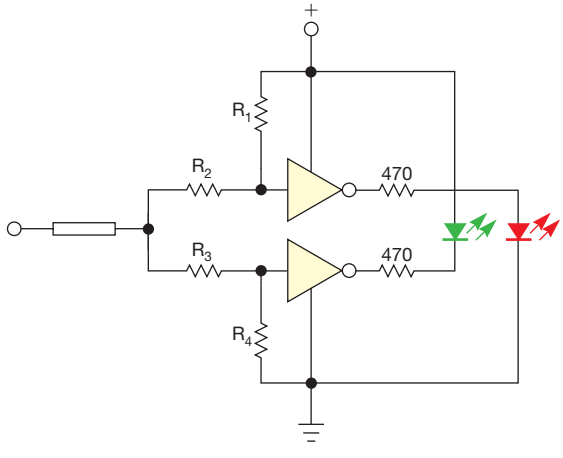

Figure 1 You can make a logic probe TTL/CMOS-compatible using just two gates from a single unit of an HD14069UB hex inverter. The suggested values for threshold and supply voltages are 2.5 and 5V, respectively; those for R_1, R_2, R_3, and R_4 are 1 MΩ, 680 kΩ, 200 kΩ, and 1 MΩ, respectively.

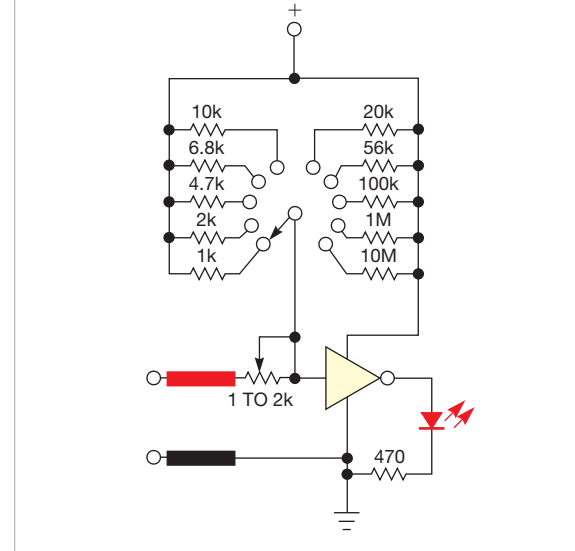

Figure 2 This single-gate continuity tester has an adjustable detection threshold.

should be set so that the LED just goes off. This method results in a compact arrangement, which a small package can accommodate. Another variable resistor (1 to 2 kΩ) is included in series with the negative probe to make it possible to have a threshold-continuity resistance of approximately 100Ω or less. You can also use a lower transition threshold voltage for the gate by including a couple of diodes followed by a 10-kΩ load resistor to ground in series with the positive supply rail. This arrangement can also be used to test for live ac-mains lines (**Reference 3**) with suitable modification, virtually making five gadgets.

Three gates still remain in the 4069 package; you can use two of them to make an astable oscillator/monostable single-pulse-generator circuit, which a complementary bipolar pair buffers to increase the drive current (**Figure 3**). You select between a single pulse or a pulse train with an SPDT (single-pole/double-throw) switch set to P (pulse) or A (astable). In pulse mode, pressing the switch produces a brief negative-going pulse at the input to the second gate as C_2 begins charging. The resulting high at the gate output causes a positive-going pulse at the junction of Q_1 and Q_2. It also is latched, and the switch is debounced by the positive feedback through capacitor C_1, which begins charging at a time constant that the selection of R_1, R_2, or R_3 determines. When the voltage across C_1 equals the threshold voltage, the second gate output returns low, again with positive feedback through C_1, driving the second gate input high and ending the pulse.

The diode in parallel with C_2 is always reverse-biased and serves as a very large-value resistor to discharge C_2. Assuming a typical diode leakage of 1 nA, the equivalent resistance at 2.5V is about 2.5 GΩ. The RC discharge time constant of approximately 125 msec is suitable for the human rate of pushing the button.

The values of R_1 through R_3 set the astable frequency or the one-shot's pulse width. The 220-kΩ resistor at the input of the second gate is included to limit the leakage of current from the capacitor into the gate input when its voltage is below that of ground or higher than V_{DD} by 0.6V. The astable produces a frequency of approximately 1/(2.2RC), whereas the threshold voltage of the gate determines the pulse width of the one-shot, which is approximately 0.7 to 1.1RC.

It is sometimes useful to listen to an audio signal at a test-circuit point. The 4069, with its high input impedance and sufficient output drive current of approximately 6.8 mA, can drive a small PCB-mountable speaker. That approach lets you build a simple audio probe (**Figure 4**). The resistor at the gate input of **Figure 4a** protects the gate if the unit under test has voltages higher than the gate supply voltage.

Two methods of driving the acoustic transducer are shown, depending on the loudness requirements. **Figure 4a** shows a direct connection to a piezo transducer. For the louder sound of a speaker, a small resistor can be added in series with the speaker of **Figure 4b** to control volume and prevent possible speaker or transistor damage. **Figure 4c** shows an optional method of biasing the gate input for enhanced sensitivity.

The biasing voltage is given by the voltage divider network using this **equation**: $V_B=R_2V_S/(R_1+R_2)-R_2V_L(1-\xi)/(R_1+R_2)-R_2V_H\xi/(R_1+R_2)$, where V_S is the supply voltage, ξ is the duty cycle ($T_H/(T_H+T_L)$) of the input signal (assumed to be a rectangular wave), V_H is the logic-high voltage, and V_L is the logic-low voltage. A suggested value for R_1 is 1 MΩ; the user can choose

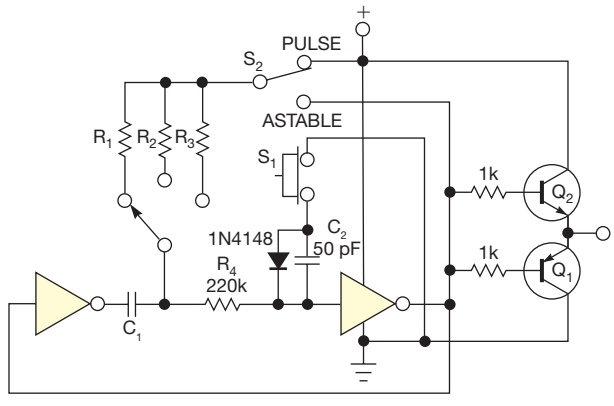

Figure 3 A complementary bipolar pair boosts the output current of the oscillator and the single-pulse generator.

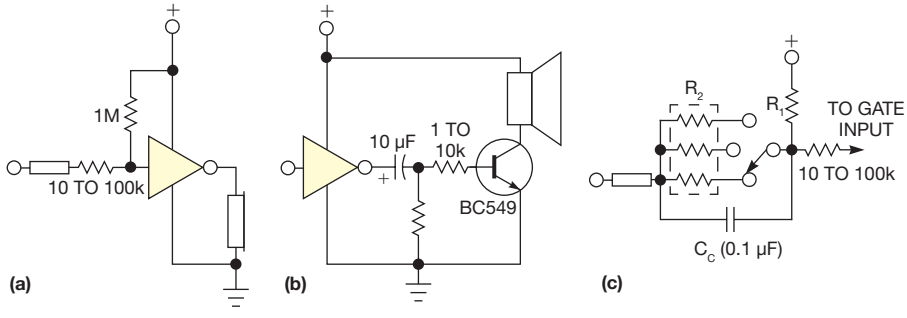

Figure 4 A resistor at the gate input protects the gate if the unit under test has voltages higher than the gate supply voltage (a). A small resistor can be added in series with the speaker to control volume and prevent possible speaker or transistor damage (b). In an optional method of biasing the gate input for enhanced sensitivity, various R_2 values are possible (c).

R_2 (suggested to be 1 MΩ) according to the **equation** for biasing voltage. Various R_2 values are possible, as the switching arrangement in **Figure 4c** shows. Capacitor C_C (suggested to be 0.1 µF) acts in series with the signal to be investigated and supplies the biasing voltage in series with the signal. The minimum strength of the signal is limited by the input threshold window of the gate and is different for different logic gates. For a rectangular signal changing between zero and the signal voltage, for example, the biasing voltage should be below the threshold window, and the value of the biasing voltage plus the signal voltage should be above the threshold window.

A stringent situation exists when those two values lie just at the edge of the window. So, for a rectangular or attenuated digital signal, $V_{SIG}=\Delta V_T$ is the minimum required signal strength. In general, gates differ in ΔV_T; some have wide widths (CD4069) and others narrow widths (CD4011). When an ac signal such as a sine wave is applied, however, the negative phase of the signal reduces the biasing voltage by its strength to V_B-V_{SIG}. It is thus sufficient that one phase produces a change equal to half of the window width. For ac signals, therefore, the minimum signal-strength criterion is $V_{SIG}=\Delta V_T/2$.

Finally, for an inverting gate, $\Delta V_T=V_{T2}-V_{T1}$, where V_{T2} is the input voltage at which the output of the gate has completely settled to logic zero, and V_{T1} is the input voltage at which the output of the gate has completely settled to logic one. R_1 and R_2 help in choosing the critical signal strength above the minimum that the threshold window of the gate has set. If R_2 is approximately 1 MΩ, then the R_2C_C time constant is 0.1 sec, which corresponds to 10 Hz and seems to be adequate.

For plain digital signals, it is enough to omit R_2 and C_C; in other words, both R_2 and C_C equal zero. It should be noted that this coupler does not remedy the stagnant signal condition, preventing a constant drain current at the output. It is intended to provide a typical transistor amplifier kind of biasing for the audio probe gate. The stagnant signal condition is taken care of with a series 10-µF capacitor at the gate output of **Figure 4b**.

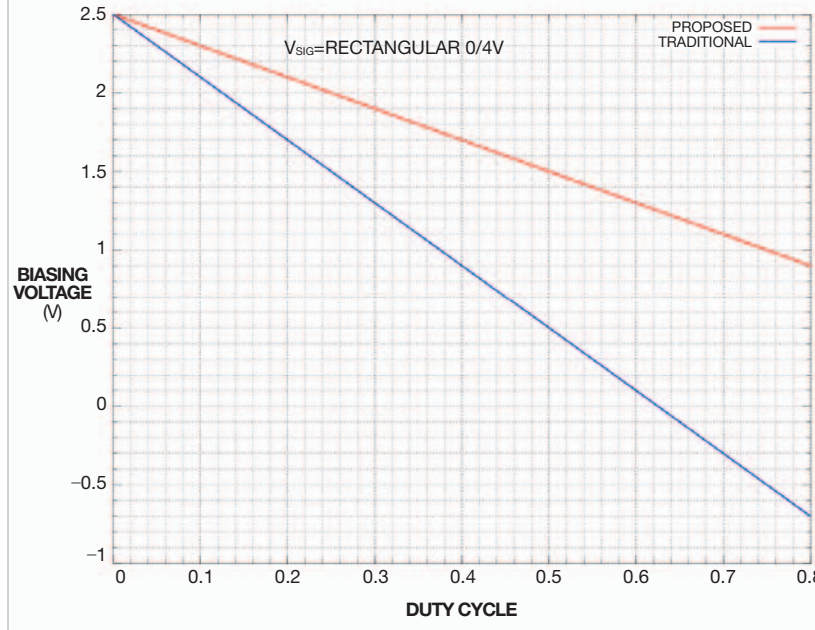

Figure 5 The input ac coupling of Figure 4c is less sensitive to duty cycle than is traditional series-capacitor ac coupling.

Readers interested in using the traditional ac coupling (with the left terminal of R_2 connected to ground instead of the probe tip) RC circuit may use the following formula to calculate the expected V'_B as a function of various parameters: $V'_B=V_SR_2/(R_1+R_2)-\xi(V_H-V_L)-V_L$, where all of the terms have the usual meaning.

Compare this **equation** with the previous **equation**. Whereas the biasing voltage in the **equation** for V'_B depends on V_H or V_L through a single multiplicative factor of the duty cycle, in the **equation** for the biasing voltage it depends on another multiplicative factor, $R_2/(R_1+R_2)<1$, thus reducing the dependence and producing a flatter profile with a duty cycle as shown in **Figure 5** for a rectangular wave of $V_L/V_H=0/4V$ and a varying duty cycle.

You can assemble all of these gadgets in a small container, such as a glue-stick tube, and use the probe for a variety of tests (**Reference 4**). You can power the probe using two 3V CR2032 lithium cells; the CMOS 4069 is a low-power device. Note, however, that 4069 devices from different manufacturers differ widely in their threshold voltages, so you should check that value before selecting a device to make the test gadgets, especially the first three.

The key to these test gadgets is the high input impedance of the CMOS gates. Other packages, such as the CD4011/4001, can also yield multiple gadgets because what matters is the use of the inverter gate.

Editor's note: In all of the circuits discussed here, the probe ground should be connected directly to the unit-under-test ground. Although the Design Idea does not discuss it, some readers might want to add CD4011/4001 NAND/NOR logic to combine the continuity tester, astable oscillator, and audio probe to provide an audio tone for the continuity tester. EDN

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